

WHAT IS CLAIMED IS:

1. A complementary metal oxide semiconductor (CMOS) image sensor comprising at least:

a non-single-crystal-silicone-base substrate;

5 an opaque layer, formed on the non-single-crystal-silicone-base substrate;

a polysilicon layer, formed on the opaque layer, the polysilicon layer comprising a charge-generating region;

10 a source and a drain, formed in the polysilicon layer, wherein a pre-channel region is formed in the polysilicon layer between the source and the drain, and the source is located between the charge-generating region and the pre-channel region;

a gate dielectric layer, formed on the polysilicon layer; and

15 a first transparent gate electrode and a second transparent gate electrode, formed on the gate dielectric layer and respectively located above the charge-generating region and the pre-channel region.

2. The image sensor according to claim 1 further comprising:

an interlayer dielectric layer, formed on the gate dielectric layer and covering the first and the second transparent electrodes, the interlayer dielectric layer comprising a first opening;

- 5 a first metal electrode, which fills the first opening and is coupled to the gate dielectric layer;

a passivation layer, formed on the interlayer dielectric layer and covering the first metal electrode, the passivation layer comprising a second opening and a third opening, respectively located above the source and the drain; and

a second metal electrode and a third metal electrode, formed on a part of the passivation layer, and respectively formed in the second opening and the third opening to be connected with a part of the interlayer dielectric layer at two sides of the second transparent gate electrode.

- 15 3. The image sensor according to claim 1, wherein the first transparent gate electrode is made of indium tin oxide (ITO).

4. The image sensor according to claim 1, wherein the second

transparent gate electrode is made of ITO.

5. A complementary metal oxide semiconductor (CMOS) image sensor comprising at least:

a non-single-crystal-silicone-base substrate;

5 an opaque layer, formed on the sides and the bottom of the non-single-crystal-silicone-base substrate;

a polysilicon layer, formed on the non-single-crystal-silicone-base substrate;

10 a source and a drain, formed in the polysilicon layer, wherein a pre-channel region is formed in the polysilicon layer between the source and the drain;

a charge-generating region, formed in the polysilicon layer, wherein the source is located between the charge-generating region and the pre-channel region;

15 a gate dielectric layer, formed on the polysilicon layer; and

a first transparent gate electrode and a second transparent gate

electrode, formed on the gate dielectric layer and respectively located above the charge-generating region and the pre-channel region.

6. The image sensor according to claim 5 further comprising:

an interlayer dielectric layer, formed on the gate dielectric layer and covering the first and the second transparent electrodes, the interlayer dielectric layer comprising a first opening;

a first metal electrode, which fills the first opening and is connected with the gate dielectric layer;

a passivation layer, formed on the interlayer dielectric layer and covering the first metal electrode, the passivation layer comprising a second opening and a third opening, respectively located above the source and the drain; and

a second metal electrode and a third metal electrode, formed on a part of the passivation layer, and respectively formed in the second opening and the third opening to be connected with a part of the interlayer dielectric layer at two sides of the second transparent gate electrode.

7. The image sensor according to claim 5, wherein the first transparent

gate electrode is made of ITO.

8. The image sensor according to claim 5, wherein the second transparent gate electrode is made of ITO.

9. A method of manufacturing a complementary metal oxide semiconductor (CMOS) image sensor, comprising the steps of:

providing a non-single-crystal-silicone-base substrate;

forming an opaque layer on the non-single-crystal-silicone-base substrate;

forming a polysilicon layer on the opaque layer, wherein the polysilicon comprises a charge-generating region;

forming a source and a drain in the polysilicon layer, wherein a pre-channel region is formed in the polysilicon layer between the source and the drain, and the source is located between the pre-channel region and the charge-generating region;

forming a gate dielectric layer on the polysilicon layer; and

forming a first transparent gate electrode and a second transparent

gate electrode on the gate dielectric layer, wherein the first and the second transparent gate electrodes are respectively located above the charge-generating region and the pre-channel region.

10. The method according to claim 9, wherein the step of forming a source and a drain in the polysilicon layer further comprises the steps of:

defining the top surface of the polysilicone layer to form two pre-doping regions; and

doping the two pre-doping regions to form the source and the drain in the polysilicon layer.

11. The method according to claim 9, wherein after the step of forming a first transparent gate electrode and a second transparent gate electrode on the gate dielectric layer, the method further comprising the steps of:

forming an interlayer dielectric layer, having a first opening, on the gate dielectric layer, wherein the interlayer dielectric layer covers the first transparent gate electrode and the second transparent gate electrode, and the first opening, located between the first transparent gate electrode and the second transparent gate electrode, exposes a part of

the gate dielectric layer;

forming a first metal electrode to fill the first opening and be connected with the gate dielectric layer;

forming a passivation layer, having a second opening and a third opening, on the interlayer dielectric layer, wherein the passivation layer covers the first metal electrode, and the second opening and the third opening are respectively located above the source and the drain, and expose a part of the interlayer dielectric layer; and

forming a second metal electrode and a third metal electrode on the passivation layer, wherein the second metal electrode and the third metal electrode are respectively formed in the second opening and the third opening to be connected with parts of the interlayer dielectric layer at two sides of the second transparent gate electrode.

12. The method according to claim 9, wherein the first transparent gate electrode is made of indium tin oxide (ITO).

13. The method according to claim 9, wherein the second transparent gate electrode is made of ITO.

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